AMENDMENTS TO THE CLAIMS

Please substitute the following set of claims for all prior versions of claims. The amendments to the claims are indicated below:

1 to 13 (Cancelled).

14. (Currently Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a metal wiring layer provided on said active element;

an interlayer insulating film covering said active element;

a pad metal for an electrode pad forming an external electrical terminal for said semiconductor device, said pad metal being provided over said interlayer insulating film and substantially covering the at least two diffusion layers and said gate electrode of the active element, wherein said active element is on a side of the interlayer insulating film opposite to the pad metal and said pad metal is over the active element; and

a barrier metal layer provided over said active element and said interlayer insulating film, so that said pad metal is provided on said barrier metal layer and covering said active element, wherein:

said interlayer insulating film has at least a level difference compensating film for compensating for a level difference of the metal wiring layer, wherein said level difference compensating film is between portions of the metal wiring layer; and

~~a portion of~~ said level difference compensating film under said pad metal is substantially completely removed.

15. (Currently Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a metal wiring layer provided on said active element;

an interlayer insulating film covering said active element;

a pad metal for an electrode pad forming an external electrical terminal for said semiconductor device, said pad metal being provided over said interlayer insulating film and substantially covering the at least two diffusion layers and said gate electrode of the active element, wherein said active element is on a side of the interlayer insulating film opposite to the pad metal and said pad metal is over the active element; and

a barrier metal layer provided over said active element and said interlayer insulating film, so that said pad metal is provided on said barrier metal layer and covering said active element,

wherein:

said interlayer insulating film has at least a level difference compensating film for compensating for a level difference of the metal wiring layer, wherein said level difference compensating film ~~is disposed substantially no higher than~~ under the pad metal is not disposed over a highest portion of the metal wiring layer and said compensating film is disposed between portions of the metal wiring layer; and

said level difference compensating film is formed to a minimum thickness necessary for compensating for the level difference of the metal wiring layer.

16. (Previously Presented) The semiconductor device as set forth in claim 14, further comprising a passivation film, said passivation film being formed to cover a large part of said pad metal, and an aperture in said passivation film having an edge adjacent an inside edge of said pad metal.

17 to 21 (Cancelled).

22. (Currently Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a lower interlayer insulating film formed to cover said active element;

a metal wiring layer provided on said lower interlayer insulating film;

an upper interlayer insulating film having a third layer formed to cover said metal wiring layer; and

a pad metal for an electrode pad forming an external electrical terminal for said semiconductor device, said pad metal being provided over said upper interlayer insulating film and substantially covering the at least two diffusion layers and a gate electrode of the active element, wherein said active element is on a side of the upper and lower interlayer insulating films opposite to the pad metal, and said pad metal is over the active element;

another metal wiring layer formed over the active element;

wherein each of said lower and upper interlayer insulating films have a trilaminar structure, each of a first layer and ~~a~~ the third layer of the trilaminar film being a silicon nitride film or a silicon oxide film, while a second layer of the trilaminar film being formed of spin-on-glass, and

the second layer of the upper interlayer insulating film formed to a minimum thickness necessary for compensating the level difference of the another metal wiring layer and wherein said second layer of the upper interlayer insulating film under the pad metal is not disposed over ~~is disposed substantially no higher than~~ a highest portion of the another metal wiring layer and is ~~between~~ disposed between portions of the another metal wiring layer, wherein the second layer is below the third layer of the upper interlayer insulting film.

23 to 24 (Cancelled).

25. (Currently Amended) A semiconductor device, comprising:

an active element provided on a semiconductor substrate, said active element including at least two diffusion layers and a gate electrode;

a first metal wiring layer formed over the active element;

a plurality of other metal wiring layers above said active element; and

a plurality of interlayer insulating films each being provided between a pair of said metal wiring layers, wherein said plurality of interlayer insulating films and plurality of metal wiring layers are vertically aligned above the active element;

wherein each interlayer insulating film has a multilayer structure including at least a spin-on-glass film sandwiched between insulating films formed of a silicon nitride film or a silicon oxide film;

further wherein the film formed of spin-on-glass in the interlayer insulating film is formed to a minimum thickness necessary for compensating for a level difference of one of said metal wiring layers and wherein the spin-on-glass film is between the one of said metal wiring layers and said spin-on-glass film is disposed under the pad metal so as to not cover ~~substantially no higher than~~ a highest level of the one of said metal wiring layers;

a pad metal for an electrode pad forming an external electrical terminal for said semiconductor device, said pad metal being provided over said interlayer insulating films and over the active element.

26. (Previously Presented) The semiconductor device as in claim 25 wherein the pad metal substantially covers at least two diffusion layers and said gate electrode of the active element, wherein said active element is on a side of the interlayer insulating film opposite to the pad metal.

27. (Previously Presented) The semiconductor device as in claim 16, further comprising another barrier metal layer, said another barrier metal layer is provided on the passivation film and the pad metal which is exposed by a window in the passivation film.

28. (Previously Presented) The semiconductor device as set forth in claim 14, wherein said pad metal is connected to said metal wiring layer via a through-hole in said

interlayer insulating film, wherein the through-hole does not penetrate the level difference compensating film.

29. (Previously Presented) The semiconductor device as set forth in claim 15, wherein said pad metal is connected to said metal wiring layer via a through-hole in said interlayer insulating film, wherein the through-hole does not penetrate the level difference compensating film.

30. (Previously Presented) The semiconductor device as set forth in claim 22, wherein

said another metal wiring layer is connected to the at least two diffusion layers, and also connected, via a through-hole, to said metal wiring layer provided on said lower interlayer insulating film

said pad metal is connected to said metal wiring layer via a through-hole made at sad upper interlayer insulating film, and

the respective through-holes in said upper and lower interlayer insulating films do not penetrate respective second films of said upper and lower interlayer insulating films.

31. (Previously Presented) The semiconductor device as set forth in claim 25 wherein

said first metal wiring layer is connected to the at least two diffusion layers,

a pair of upper and lower metal wiring layers of said metal wiring layers are connected to each other via a through-hole, each interlayer insulating film having the through-hole, and

the through-hole is formed so as not to penetrate a spin-on-glass of each interlayer insulating film.

32. (Currently Amended) The semiconductor device as set forth in claim 15 wherein the interlayer insulating film further comprises a first layer and said level difference compensating film is ~~in a plane common to the metal wiring layer~~ coplanar with a highest portion of the first layer of the interlayer insulating film.

33. (Currently Amended) The semiconductor device as set forth in claim 22 wherein the second layer of the upper interlayer insulting film is ~~in a plane common to the another metal wiring layer~~ coplanar with a highest portion of the first layer of said upper interlayer insulating film.

34. (Currently Amended) The semiconductor device as set forth in claim 25 wherein the spin-on-glass film is ~~in a plane common to the one of said wiring layers~~ coplanar with a highest portion of a lower one of said silicon nitride film and said silicon oxide film of the interlayer insulating film.